An investigation into the role of LET and supply voltage in determining the critical charge for Single Event Upset in a 65-nm CMOS SRAM

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Abstract

Continuous downscaling of CMOS technology results in a decrease in minimum charge ($Q_{critical}$) upsetting the logic state of a memory cell which are mainly attributed to the lower supply voltage. In this paper, the $Q_{critical}$ required to cause upset in a 6T SRAM cell designed in 65-nm process is investigated in three different supply voltages. To this purpose, a memory cell was designed using the Mixed-Mode and Victory modules of Silvaco TCAD tool. Then, the variations in output voltages were studied after striking charged particles with different values of Linear Energy Transfer (LET). The $Q_{critical}$ was obtained by integrating the output current when the output voltages were inverted. The results showed that lowering in supply voltages has been led to a decrease in $Q_{critical}$.

Keywords: Single Event Upset, Critical Charge, Linear Energy Transfer, Supply Voltage

Introduction

Nowadays, microelectronic devices are widely used in environments with high levels of ionizing radiation such as space. Rapid downscaling of these devices into sub-micron technologies, made them become more sensitive to radiation. When the electronic devices are exposed to radiation, they may lose their correct operation due to two types of radiation effects, cumulative or Single Event Effects (SEE). SEEs unlike the cumulative effects refer to the phenomenon in which a single particle causes abrupt changes or transient behavior in the device or circuit. Single Event Upsets (SEU) as the most common events can abruptly change the logic state of the microelectronic device such as memory. The minimum collected charge needed to flip the logic state of the device is called critical charge ($Q_{critical}$) which is a criterion of SEU vulnerability. Due to smaller node capacitance and lower supply voltage in new nanometer technologies, the critical charge is relatively small. A widely used microelectronic device that is prone to SEU is SRAM. The most common type of SRAMs used in commercial applications are consist of 6 MOSFETs. Figure 1, shows a schematic of 6T (6 Transistor) SRAM cell in which M_5-M_6 are access transistors for reading and writing operations, while M_1-M_2 and M_3-M_4 form two interconnected inverters for storing the data. Each inverter has been composed of NMOS and PMOS. The outputs of inverters are connected to each other's input. When the incident particle strikes on one of the inverters, it produces a transient change in the voltage appearing at the input of the other inverter. If this voltage falls below a threshold for switching the inverter, the logic state of memory cell will change. In this study, calculations have been performed to indicate the voltage supply (V_{DD}) influence on the $Q_{critical}$ induced by incident particles irradiation with different values of LET for a 65-nm CMOS SRAM cell.

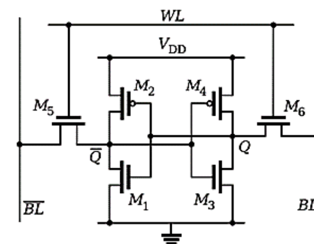

Figure 1. Schematic of an SRAM memory cell.

Materials & methods

In the approach used in this work, to determine the $Q_{critical}$, one of the SRAM cells was simulated using mixed-mode and Victory modules of Silvaco TCAD tool. Victory modules have been utilized to perform 3D simulations of the transistor that beam has struck on it. In order to reduce the time of calculations, remaining transistors were described as circuit elements using Mixed-Mode module. According to reference [1], NMOS is more sensitive than PMOS. So, a 3D model was proposed based on 65-nm technology for NMOS. To ensure the accuracy of the model, the characteristic curve of I_d-V_g, extracted and calibrated according to reference [1]. When incident particle passes through a semiconductor material, electron-hole pairs released along its path. The mean amount of energy loss per unit distance by the impinging particle is called Linear Energy Transfer (LET). In order to determine the $Q_{critical}$, the incident particle beam with different values of LET was irradiated to the NMOS with three different supply voltages (0.85 V, 1.1 V and 1.3 V) and the output voltage variations were considered. The results are discussed in the next section.

Results and discussion

Figure 2 presents a comparison between the data obtained for I_d-V_g curves in our designed NMOS and the results in reference [1]. As can be observed, the graphs are in good agreement. In the both graphs, the drain bias is applied 0.1 V and gate bias varies from 0- 2.5 V. The Threshold voltage (V_{th}) is the main parameter that determines whether a transistor works or not. According to ITRS (International Technology Roadmap for Semiconductors), V_{th} should be in the range of 0.176 V to 0.225 V for 65-nm technology. In this work, the value for V_{th} has been achieved 0.183 V which is in-line with ITRS guideline. Figure 3 illustrates the output voltages Q & $\bar{Q}$ (in Figure 1) of the cell just for supply voltage of 1.1 V, which are calculated for two values of LET=1 MeV.cm^2/mg and LET=1.2 MeV.cm^2/mg. As can be observed the SRAM cell flips when the LET is 1.2 MeV.cm^2/mg. The output current has been shown in Figure 4. The critical charge is calculated by integrating the output current over the time interval that the logic state of output voltage changes. As can be seen in Figure 4, the critical charge is the specified area under the curve. Calculation of this area resulted in 1.48 fC for critical charge for supply voltage of 1.1 V. The value of critical charge reported in reference [2] for an SRAM with a similar specification is 1.35 fC. There is a reasonable consistent in the results. The precedure mentioned above, has been applied for determining of critical charge for supply voltages of 0.85 V and also 1.3 V. the results have been shown in Table 1.

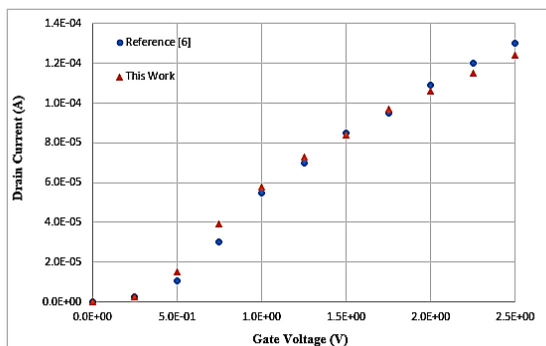

Figure 2. A comparison between I_d-V_g curve for the calibrated NMOS in this work and reference [1].

Table 1. The calculated critical charge for various supply voltages

V_{DD} (V)	Critical Charge (fC)
0.85	1.01
1.10	1.48
1.30	1.62

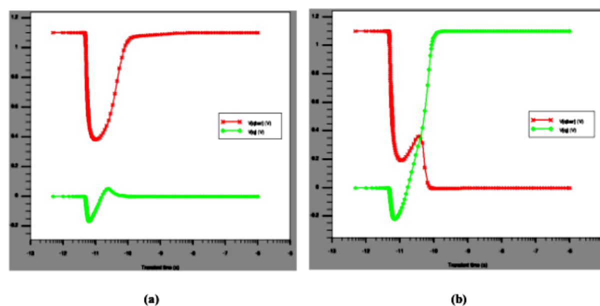

Figure 3. Variations in output voltages (Q & $\bar{Q}$) in V_{DD}=1.1 V for (a) LET=1 MeV.cm^2/mg , (b) LET=1.2 MeV.cm^2/mg

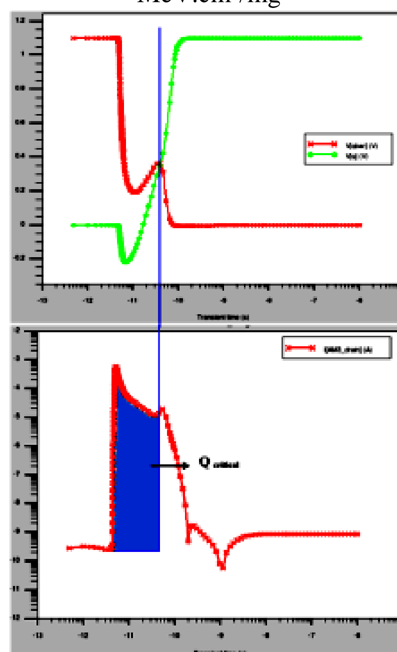

Figure 4. Determination of critical charge when the logic state of output inverted.

Conclusions

SEUs are the major threat to system reliability in today's nanometer technologies. In this paper, we characterized the critical charge of a 6T SRAM cell designed in the 65-nm process using TCAD simulations. the results showed a reasonable agreement with other data in the litrature. Due to the decrease of capacitances in new nanometer technologies, the simulation results revealed that lowering the supply voltage reduced the critical charge and making the new technologies more susceptible to SEUs.

References

[1] P. KUMAR, M. Vashishath, and P. K. Bansal, in *An Investigation into NMOS at 65 nm using Silvaco TCAD.* International Journal Management, Technology and Engineering, (2018).

[2] Y. Bing et al., *Impact of energy straggle on proton-induced single event upset test in a 65-nm SRAM cell,* Chin. Phys. B, 26(8), (2017) p.088501.